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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/905,398
Filing Date: July 14, 2001
Appellant(s): LAYADI ET AL.

James H. Beusse
Reg. No. 27,115
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed August 31, 2005 appealing from the Office action mailed April 14, 2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,231,306	Meikle et al.	7-1993
JP-08-107148	Yamashita	4-1996
6,211,072	Brennan	4-2001

S. Wolf et al., "Silicon Processing for the VLSI Era" Lattice Press, Vol. 1, (1986), pp. 407-409.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-5, 7 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al., (JP. Patent No. 08-107148) in view of Meikle et al., (U.S. Patent No. 5,231,306) (all of record).

With respect to claim 1, insofar as the structure is concerned, Yamashita teaches a semiconductor device substantially as claimed including:

a substrate (21) having a device feature (22-27) formed thereon;

a dielectric layer (28) disposed over the substrate (21) and device feature (22-27) and having at least one contact hole (29) formed therein;

a conductive layer (30) disposed over the dielectric layer (28) and extending within the contact hole (29);

a layer of metal (31) disposed over the polish stop layer (30) within the contact hole (29) and formed a plug; and

wherein the conductive layer (30) comprises titanium nitride (TiN). (See Fig. 7, [0031]-[0037]).

Thus, Yamashita is shown to teach all the features of the claim with the exception of using TiAlN for the conductive layer (30).

However, Meikle teaches that TiAlN are known in the art to be used in place of TiN in semiconductor devices. (See Abstract of Meikle).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the polish stop layer (30) of Yamashita using TiAlN as taught by Meikle because TiAlN is more resistant to diffusion than TiN, can be etched and sputter like TiN, has better thermal budget and better stability on silicon; thus, can replace TiN in many of its uses in semiconductor device. (See abstract of Meikle).

Product by process limitation:

The expression "polish stop layer" is/are taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no

matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. In the instant case, layer 18 is determined to be a conductive layer.

Note that Applicant has burden of proof in such cases as the above case law makes clear.

With respect to claim 2, the semiconductor device of Yamashita further includes a metal coating (27) under the dielectric layer (28), the metal coating (27) comprises titanium nitride.

Note that, as discussed previously, in view of Meikle, metal compound of titanium, nitride and aluminum (TiAlN) can be used in place of the TiN layer (27).

With respect to claim 3, the dielectric layer (28) of Yamashita comprises SiO_2.

With respect to claim 4, the metal coating (27) of Yamashita comprises an ARC.

With respect to claims 5 and 7, the barrier layer of Meikle comprises TiAlN and appears to have aluminum percentage (1%-20%) weight as claimed.

With respect to claim 21, insofar as the structure is concerned, Yamashita teaches a semiconductor device substantially as claimed including:

a metal layer (25) disposed on a substrate (21);

a barrier layer (27) disposed on the metal layer (25);

a dielectric layer (28) disposed on the barrier layer (27);

a patterned layer of photoresist (not shown) disposed on the dielectric layer (28) exposing a selected portion of the dielectric layer (28);

wherein the barrier layer (27) function as an etch stop layer upon removal of the selected portion of the dielectric layer (28) to prevent the etching process from compromising the underlying metal layer (25). (See Fig. 4, [0031]-[0033]).

Thus, Yamashita is shown to teach all the features of the claim with the exception of using TiAlN for the barrier layer (27).

However, Meikle teaches that titanium aluminum nitride (TiAlN) are known in the art to be used in place of barrier layer (TiN) in semiconductor devices. (See Abstract of Meikle).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the polish stop layer (30) of Yamashita using TiAlN as taught by Meikle as described above with respect to claim 1.

Note that, the barrier layer (27) of Yamashita, in view of Meikle, functions as an etch stop layer, thus, upon removal of the selected portion of the dielectric layer (28), the barrier layer (27) prevents the etching process from compromising the underlying metal layer.

With respect to the patterned photoresist layer (not shown), Yamashita teaches: "furthermore, the contact hole 29 which reaches said Si oxide film 28 at said TiN thin film 27 is formed through resist (illustration abbreviation) spreading, exposure, and etching with the usual lithography technique and dry etching techniques (the RIE method, etc.)" (See [0033]).

The formation of the patterned photoresist is well known in the art. (See S. Wolf et al. *Silicon Processing for the VLSI Era.* Vol. 1, pp. 407-409).

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 19 and 20 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Brennan (U.S. Patent No. 6,211,072) of record.

With respect to claim 19, insofar as the structure is concerned, Brennan teaches semiconductor structure as claimed including:

a substrate layer (12);

a dielectric layer (20) disposed over the substrate layer (12) and having a via (24) formed therein;

a polish stop layer (28) comprising titanium nitride alloyed with carbon disposed over the dielectric layer (20) and extending into the via (24); and

a metal layer (26) disposed over the polish stop layer (28) and filling the via (24). (See Fig. 5).

With respect to the hardness of the titanium nitride alloyed with carbon (28) as compared to that of titanium nitride material, since the TiCN (28) of Brennan is titanium nitride alloyed with carbon, the TiCN layer (28) of Brennan inherently has the hardness as claimed.

Further, since the TiCN layer (28) of Brennan comprises a same material as claimed (titanium nitride alloyed with carbon), it would function the same.

With respect to claim 20, the percentage weight of carbon in the TiCN layer (5%) of Brennan is within the claimed range (5 to 20 %).

(10) Response to Argument

With respect to claims 19-20, which are not appealed, these claims stand rejected as shown above.

Rejection of claims 1-5, 7 and 21 under 35 U.S.C. 103(a):

Appellants indicate that: "a polish stop layer is not used in semiconductor devices but is rather used in the fabrication of semiconductor devices".

It is respectfully submitted that both uses are accurate: the polish stop layer is used for forming the semiconductor device and the polish stop layer remaining on the semiconductor device is used as an integral part of the contact structure as clearly seen in Fig. 8 of Yamashita, where conductive barrier layer 30 is the etch stop layer.

Further, in response to Appellant's argument that Yamashita's polish stop layer is not being utilized in semiconductor devices, it is respectfully submitted that the TiN polish stop layer 30 is part of the semiconductor device as clearly seen in Fig. 7, where subsequent structures (e.g. 31, 32, 33) are formed over the polish top layer 30.

Furthermore, the term "polish stop" is determined to be a process limitation, while the claims are directed to a semiconductor device.

Appellants further argue: "[t]he mere fact that references can be combined or modified in hindsight does not render that resultant combination obvious. Rather, the prior art must also suggest the desirability of the combination (In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990))".

The prior art (Meikle) clearly suggests: "[t]he TiAlN material is more resistant to diffusion than TiN and can be etched and sputtered like TiN. It has better thermal budget than TiN and better stability on silicon, and thus can replace TiN in many of its uses in semiconductor devices". (See the Abstract).

Appellants assert: "[f]or example, tungsten serves well as a filament in a light while aluminum quickly is destroyed. Yet both of these are electrical conductors and are used as such in semiconductor structures. The examiner's logic would suggest that aluminum could function as a light filament since it can be used as an electrical conductor".

The logic here is that TiN may be replaced with TiAlN for the same purpose and in the same environment. There is nothing in the prosecution relating to light filaments.

The suggestion to combine is clearly indicated by the prior art itself, which is the strongest form of motivation. The factual evidence of MPEP 2142 clearly satisfied. The prima facie case of obviousness has been established.

In response to Appellant's argument that the references fail to show certain features of Appellant's invention, it is noted that the features upon which Appellant relies i.e., Applicant teaches the use of TiAlN during the stage of Chemical Mechanical Planarization (CMP) for fabricating a semiconductor device, are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Further, in response to Appellant's argument that the references fail to show certain features of Appellant's invention, it is noted that the features upon which Appellant relies, i.e., Applicant uses TiAlN during the process of fabricating a semiconductor device, while Meikle uses TiAlN to ultimately operate within a finished semiconductor device, are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations

from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claims 1 and 21 are drawn to semiconductor device. Appellant's purported distinctions between the present invention and the applied references relate to manufacturing process limitations, which limitation are not in claims before the Board.

Regarding the reasonable expectation of success, Meikle clearly suggests: "TiAlN can replace TiN in many of its uses in semiconductor devices". Meikle further adds: "the invention allows the use of conventional techniques to deposit the barrier film in high aspect ratio contacts". (Col. 2, lines 53-55).

The high aspect ratio contacts as indicated by Meikle is similar to the contact hole (29) of Yamashita. Therefore, it would have been obvious to one of ordinary skill that the TiAlN of Meikle can be formed on the dielectric layer (28) and extend within the contact hole (29) in place of the TiN of Yamashita.

In response to Appellants' argument that Meikle teaches TiAlN is more resistant to diffusion than TiN provides no motivation for using titanium nitride alloyed with aluminum in place of titanium nitride as a polish stop layer, the fact that Appellants has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). Further, there is nothing to indicate that diffusion through TiN is necessary or desired by Yamashita.

Referring to Fig. 5 of Yamashita, Appellants conclude: "[t]hus, Yamashita actually teaches that the material of layer 27, which is titanium nitride, will not function as an etch stop layer".

Actually, in Fig. 5, the titanium nitride layer (27) of Yamashita is intentionally etched. However, in Fig. 4, the titanium nitride (27) clearly functions as an etch stop layer, since the etching of layer 28 to form opening 29 stops at TiN layer 27, thus the term "etch stop layer". This is similar to Fig. 4 of the instant application.

Appellants finally conclude: "[t]hus, the combination of the teaching of Meikle into the device of Yamashita would not result in the intended structure of FIG. 6 of Yamashita, thereby destroying the intent of the Yamashita patent".

However, as discussed above, claim 1 recites: a polish stop layer disposed over the dielectric layer and extending within the contact hole. Clearly the limitation is taught in Fig. 6 of Yamashita, where the polish stop layer (27) is disposed over the dielectric layer (28) and extending within the contact hole (29). Therefore, it is obvious to use the TiAlN of Meikle, for the TiN (27) of Yamashita, as discussed above. This is nothing more than the simple substitution of one material for another in the same environment and for the same purpose.

Thus, the conclusion of destroying the intent of the Yamashita patent is erroneous.

Finally, with respect to claim 21, Appellants state: "[c]laim 21 includes the limitations of "a layer of titanium aluminum nitride disposed on the metal layer" and "wherein the layer of titanium aluminum nitride function as an etch stop layer upon removal of the selected portion of

the dielectric layer to prevent the etching process from compromising the underlying metal layer". Then Appellants conclude: "[t]he combination of Yamashita and Meikle fails to establish a prima facie case for the obviousness of this claimed combination".

As discussed previously, using TiAlN in place of TiN have been suggested by Meikle. Therefore, the combination of Meikle and Yamashita rendered claim 21 obvious.

Appellants cite numerous case law and assert: "[t]he Applicant is aware of no prior art that suggests a reasonable likelihood of success associated with the combination of titanium, aluminum and nitride in a polish stop layer".

All of the cited case law can be summarized as:

A) Does the combination of the references result in all limitation as claimed ?

Yes, all limitations of claim 21 are covered.

B) Are there suggestion and motivation to combine ?

Yes, the suggestions and motivations are clearly offered by the prior art, Meikle.

C) Are there expectation of success ?

Yes, since TiAlN can be deposited with all of the conventional techniques that used to form TiN. TiN of Yamashita can be easily replaced with TiAlN of Meikle. Therefore, reasonable expectation of success is clearly established.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

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LITHOGRAPHY I :

OPTICAL PHOTORESIST MATERIALS

and PROCESS TECHNOLOGY

Microcircuit fabrication requires that precisely controlled quantities of impurities be introduced into tiny regions of the silicon substrate, and subsequently these regions must be interconnected to create components and VLSI circuits. The patterns that define such regions are created by lithographic processes. That is, layers of photoresist materials are first spin-coated onto the wafer substrate. Next, the resist layer is selectively exposed to a form of radiation, such as ultraviolet light, electrons, or x-rays. An exposure tool and mask, or data tape in electron beam lithography, are used to effect the desired selective exposure. The patterns in the resist are formed when the wafer undergoes the subsequent "development" step. The areas of resist remaining after development protect the substrate regions which they cover. Locations from which resist has been removed can be subjected to a variety of additive (e.g. lift-off) or subtractive (e.g. etching) processes that transfer the pattern onto the substrate surface.

Three chapters are devoted to the details of lithographic processing for VLSI. The first is concerned with the properties of photoresist materials, and the resist processing technology utilized in VLSI fabrication. The discussion is restricted to resists exposed by optical (e.g. UV) radiation. The subject of the second chapter deals with the tools used to expose the resist. That is, optical aligning equipment and photomasks are described. The third chapter covers advanced lithography, including electron beam, ion beam, and x-ray patterning technology.

BASIC PHOTORESIST TERMINOLOGY

The basic steps of the lithographic process are shown in Fig. 1. The photoresist (PR) is applied as a thin film to the substrate (e.g. SiO_2 on Si), and subsequently exposed through a *mask* (or *reticle* in step-and repeat projection systems). The mask contains clear and opaque features that define the pattern to be created in the PR layer. The areas in the PR exposed to the light are made either soluble or insoluble in a specific solvent known as a *developer*. In the case when the irradiated (exposed) regions are soluble, a positive image of the mask is produced in the resist. Such material is therefore termed a *positive* resist. On the other hand, if the *nonirradiated* regions are dissolved by the developer, a negative image results. Hence the resist is termed a *negative* resist. Following development, the regions of SiO_2 no longer covered by resist,

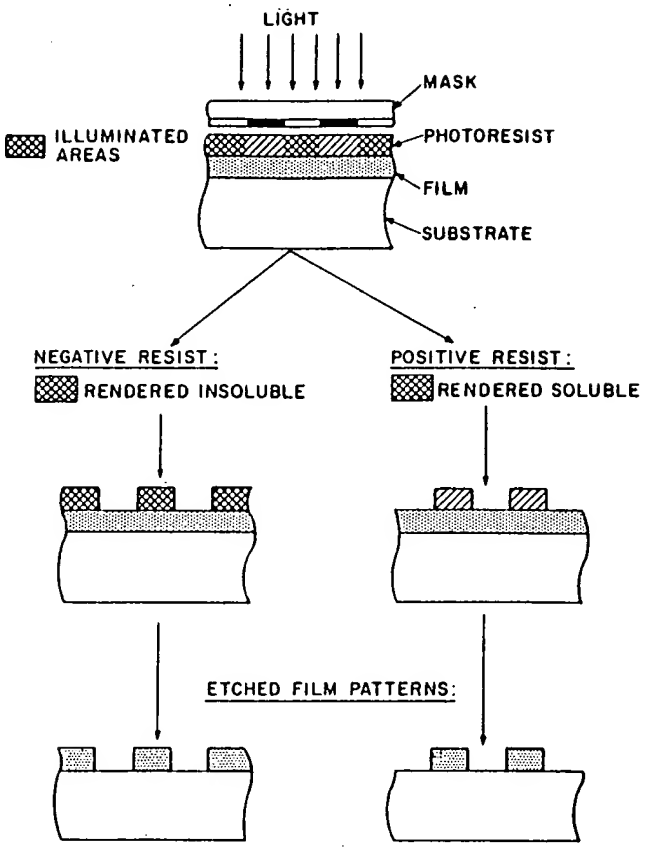

Fig. 1 Exposure and development of negative and positive photoresists, and the resulting etched film patterns. From L. Maissel and R. Glang. Eds. *Handbook of Thin Film Technology,* 1970. Reprinted with permission of McGraw-Hill Book Company.

are removed by etching, thereby replicating the mask pattern in that oxide layer.

The resist is seen to perform two roles in this process. First, it must respond to exposing radiation in such a way that the *mask image* can be replicated in the resist. Second, the remaining areas of resist must protect the underlying substrate during subsequent processing. In fact, the name *resist* evolved from the ability of these materials to "resist" etchants.

Although both negative and positive optical resists are used to manufacture semiconductor components, the higher resolution capabilities of positive resists have virtually made them the exclusive choice for VLSI applications. As such, almost all of the discussion in this chapter will be limited to positive resists and their processing. Conventional positive optical lithographic processes and resists are capable of producing images on VLSI substrates with dimensions as small as 0.8-1.5 μm. For submicron features, however, diffraction effects during exposure may ultimately cause other higher resolution techniques to replace optical lithography.

In general, users of resists are not overly concerned with the complexities of resist chemistry, but rather how well the resist will function in their process. The majority of the information in this chapter is presented in this vein.

Conventional optical photoresists are three-component materials, consisting of: a) the matrix material (also called *resin*), which serves as a binder, and establishes the mechanical properties of the film; b) the sensitizer (also called the *inhibitor*), which is a photoactive compound (PAC); and c) the solvent (different than the developer solvent),which keeps the resist in the liquid state until it is applied to the substrate being processed. The *matrix material* is usually inert to the incident imaging radiation. That is, it does not undergo chemical change upon irradiation, but provides the resist film with its adhesion and etch resistance. It also deter-

mines other film properties of the resist such as thickness, flexibility, and thermal flow stability.

The *sensitizer* is the component of the resist material that reacts in response to the actinic radiation. The term *actinic* relates to the property of radiant energy (especially in the visible and ultraviolet regions) by which photochemical changes are produced. The sensitizer gives the resist its developer resistance and radiation absorption properties.

PHOTORESIST MATERIAL PARAMETERS

As previously indicated, photoresist performs two primary functions: 1) precise pattern formation; and 2) protection of the substrate during etch. A large group of material properties possessed by the resist play a role in how effectively these functions are performed. The material parameters can be grouped into three categories: a) *optical properties*, including, resolution, photosensitivity, and index of refraction; b) *mechanical /chemical properties*, including, solids content, viscosity, adhesion, etch resistance, thermal stability, flow characteristics, and sensitivity to ambient (e.g. oxygen) gases; and c) *processing and safety related properties*, including, cleanliness (particle count), metals content, process latitude, shelf life, flashpoint, and threshold limit value (TLV, a measure of toxicity). In this section we discuss these parameters. By understanding the role that each parameter must fulfill to allow the resist to function effectively, users can better select and match resists to their particular applications[1,2,3]. Methods for measuring the values of most of the parameters are also given.

Resolution

The resolution of a lithographic process is formally defined in Chap. 13 in terms of the *modulation transfer function* of the lithography exposure equipment and how well it is matched to the resist being utilized. The term, however, is also less formally, but still widely used in the industry in a more practical sense, to *specify the consistent ability to print minimum size images under conditions of reasonable manufacturing variation.* Thus, it is fair to say that in order to build devices with submicron features, lithographic processes with submicron resolution

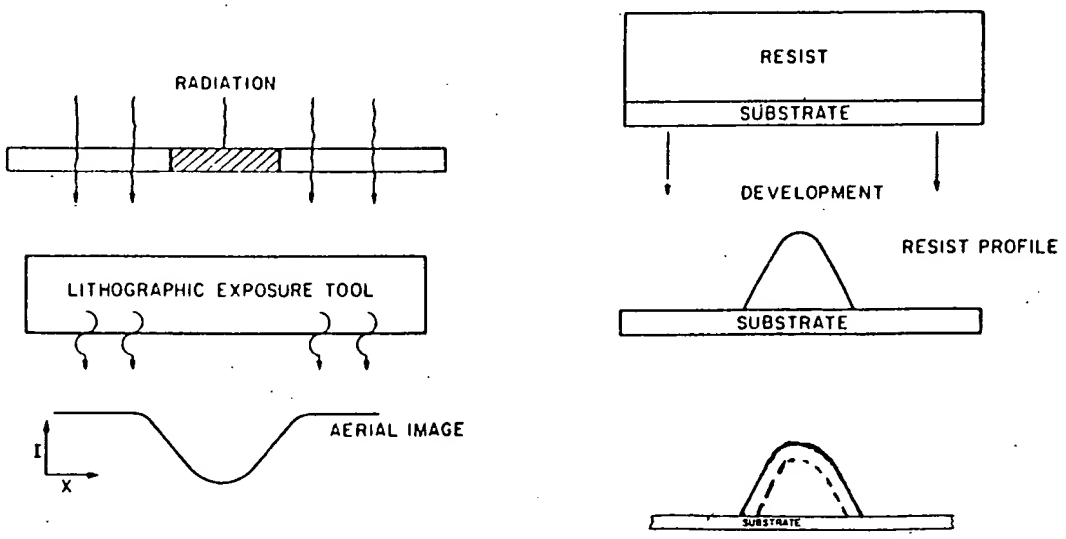

Fig. 2 Idealized photolithographic system. Final drawing shows resist profile (——) before and (- - -) after an anisotropic etch[5]. Reprinted with permission of Academic Press.